5   METHODS FOR ENHANCING CAPACITORS HAVING ROUGHENED FEATURES TO
INCREASE CHARGE-STORAGE CAPACITY

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a continuation-in-part of my prior application Serial No. 09/692,897, filed

10   October 19, 2000, which is a divisional of U.S. Patent No. 6,225,157, issued on May 1, 2001,

which is a divisional of U.S. Patent No. 6,150,706, issued on November 21, 2000. Other related

patents and applications include U.S. Patent No. 5,969,983, issued on October 19, 1999, which is

a divisional of U.S. Patent No. 6,150,706; application Serial No. 09/353,576, filed on July 15,

1999, which is a divisional of U.S. Patent No. 6,150,706; and application Serial No. 09/353,574,

15   filed on July 15, 1999, which is a divisional of U.S. Patent No. 6,150,706.

TECHNICAL FIELD

The invention relates generally to integrated circuits and more specifically to an

integrated circuit capacitor having a barrier layer that forms at least a portion of at least one of

20   the capacitor electrodes, and to an improved barrier layer.

BACKGROUND OF THE INVENTION

To increase storage density (the ratio of storage capacity to die size) and data-

access speed, dynamic-random-access-memory (DRAM) manufacturers continue to reduce the

25   geometries of and otherwise improve the structures and components that compose a DRAM

circuit. One such component is the capacitor that is used as the storage element of a DRAM cell

and one such structure is a diffusion barrier layer. Another such component is an antifuse, which

often has a structure that is similar or identical to that of a capacitor.

Unfortunately, leakage and depletion often prevent DRAM manufacturers from

30   shrinking the size of a DRAM-cell capacitor from its present size. Generally, leakage denotes

the discharge current that flows through the capacitor dielectric when the capacitor is open-

circuited, and thus is a measure of how fast the charge on a capacitor will leak away. In a

capacitor with semiconductor electrodes, e.g., polysilicon, depletion denotes the affect of the

5   depletion regions that form within these electrodes when the capacitor stores a charge. As the amount of leakage or depletion increases, the capacitor's storage capacity decreases. But unfortunately, the storage capacity of a DRAM capacitor can be reduced only so much before the DRAM cell can no longer hold its state between refresh cycles, and thus can no longer store data reliably. Therefore, because the storage capacity of a capacitor is proportional to the area of the

10   capacitor plates, the area, and thus the overall size, of a DRAM capacitor often must be relatively large to compensate for the storage-capacity-robbing affects of leakage and depletion. That is, the DRAM capacitor often must be larger than it would have to be if leakage or depletion were reduced or eliminated.

Furthermore, conventional electrode material, such as polysilicon, often causes

15   the access speed of a DRAM cell to be relatively slow. Often, the resistance of an electrode formed from such a material is relatively high. Therefore, because this resistance is effectively in series with the DRAM capacitor, it causes the time constant for charging/discharging the capacitor to be relatively large, and thus causes the DRAM cell to have a relatively long read/write time.

20   Additionally, conventional barrier materials often prevent manufacturers from reducing the dimensions of a structure disposed in a barrier layer. A barrier layer is often used to prevent the dopant in one layer from diffusing into an adjacent layer during circuit processing. A popular barrier material is tungsten silicide. But unfortunately, tungsten silicide crystallizes at about 800°C and forms relatively large grains. This crystallization degrades tungsten silicide's

25   barrier properties by orders of magnitude because dopants can easily diffuse along the grain boundaries. The large grains also prevent the use of tungsten silicide with relatively narrow structures such as wordlines. That is, if the structure's width is about the same as or is less than the grain size, tungsten silicide often cannot be used. Furthermore, although it can sometimes be used as such a barrier layer, titanium nitride oxidizes easily, and thus is unsuitable for use in

30   many applications.

Moreover, conventional electrode materials may cause a circuit coupled to an antifuse to have a relatively slow access speed. An antifuse has a structure similar to that of a capacitor, but is typically used as a one-time programmable, nonvolatile storage element. For

5   example, an antifuse can be "blown" into a short-circuited state by applying a programming voltage that is high enough to break down the dielectric such that the electrodes contact each other through the dielectric. Unfortunately, the relatively high resistance of conventional electrode materials may cause a blown antifuse to have a relatively high resistance. Because the circuit coupled to the antifuse often has a parasitic capacitance associated therewith, the

10   relatively large time constant of the coupled antifuse electrodes and parasitic capacitance can cause the circuit to have a relatively slow access speed.

SUMMARY OF THE INVENTION

        An illustrative aspect of the present invention includes a semiconductor structure

15   with a rough surface having protrusions formed from an undoped silicon film.   If the semiconductor structure is a capacitor, the protrusions help to increase the surface area of one of the electrodes of the capacitor, and hence, the capacitance of the capacitor. The semiconductor structure also includes a polycrystalline surface abutting the rough surface. The polycrystalline surface helps to enhance the structural integrity of the semiconductor structure should

20   perforations exist in the rough surface.

BRIEF DESCRIPTION OF THE DRAWINGS

        Figure 1 is a cross-sectional view of a capacitor according to one embodiment of the invention.

25   Figure 2 is a cross-sectional view of a capacitor according to another embodiment of the invention.

        Figure 3 is a cross-sectional view of a transistor having a gate structure that includes a barrier layer according to an embodiment of the invention.

        Figure 4 is a schematic diagram of a DRAM cell that uses the capacitor of Figure

30   1 or Figure 2 or the transistor of Figure 3.

        Figure 5 is a block diagram of a memory circuit that can incorporate the capacitors of Figures 1 and 2, the transistor of Figure 3, or the DRAM cell of Figure 4.

5   Figure 6 is a block diagram of a computer system that incorporates the memory

circuit of Figure 5.

Figure 7 is a cross-sectional view of a conventional semiconductor structure.

Figure 8 is a cross-sectional view of a semiconductor structure according to one

embodiment of the present invention.

10   Figure 9 is a cross-sectional view of a semiconductor structure according to one

embodiment of the present invention.

Figures 10A-10G are cross-sectional views of a semiconductor structure

undergoing an in-situ processing technique according to one embodiment of the present

invention.

15   Figures 10H-10K are cross-sectional views of a semiconductor structure

undergoing an ex-situ processing technique according to one embodiment of the present

invention.

DETAILED DESCRIPTION OF THE INVENTION

20   Figure 1 is a cross-sectional view of a DRAM capacitor 10 according to one

embodiment of the invention. The capacitor 10 includes a conventional electrode 12, which is

formed from a conductive material such as polysilicon. The electrode 12 is adjacent to one side

of a conventional dielectric 14, which is formed from an insulator such as silicon dioxide, barium

strontium titanate, or tantalum pentaoxide. Another electrode 16 is adjacent to another side of

25   the dielectric 14, and is coupled to a DRAM-cell access device, such as a transistor. The

electrode 16 is formed from a barrier material, and thus may be called a barrier electrode. The

barrier electrode 16 may include conventional barrier materials, such as titanium nitride, or may

include tungsten nitride, tungsten silicon nitride, or titanium silicon nitride, which are discussed

below in conjunction with Figure 3. Furthermore, although described for use in a DRAM cell,

30   the capacitor 10 can be used for other applications and in other integrated circuits such as

microprocessors.

The barrier electrode 16 allows the capacitor 10 to be significantly smaller than a

conventional capacitor. For example, due to its relatively high work function, the barrier

5   electrode 16 increases the height of the barrier to electron flow through the dielectric 14, and thus reduces the leakage of the capacitor 10. Furthermore, because the barrier electrode 16 is not a semiconductor material like polysilicon, there is no depletion in the electrode 16. Therefore, the overall depletion associated with the capacitor 10 is significantly reduced. Also, in one embodiment, the barrier electrode 16 is thinner than a conventional electrode such as the

10   electrode 12. For example, a conventional polysilicon electrode such as the electrode 12 may be 600 Å thick, but the barrier layer 16 may be as thin as 10 to 100 Å. Additionally, the barrier electrode 16 has a significantly lower resistance than conventional electrodes such as the electrode 12, and thus reduces the series resistance of the capacitor 10. This also reduces the time constant associated with the capacitor 10, and thus increases the access speed of the DRAM

15   cell that includes the capacitor 10. Moreover, the barrier electrode 16 also prevents dopants from diffusing from another layer into the dielectric 14, and prevents dopants in the dielectric 14 from diffusing out into other layers.

In another embodiment of the capacitor 10, the electrode 12 can be formed from silicon germanium, which has a lower work function than polysilicon. Thus, such an electrode

20   12 presents a higher barrier to the electron flow through the dielectric 14 than does polysilicon, and thus further reduces the leakage of the capacitor 10.

In still another embodiment, the electrodes 12 and 16 can be reversed. That is, the electrode 16 can be formed from a conventional electrode material such as polysilicon or from silicon germanium as discussed above, and the electrode 12 can be the barrier electrode.

25   Alternatively, both the electrodes 12 and 16 can be barrier electrodes made from the same or different barrier materials. In such an embodiment, the leakage and thickness of the capacitor 10 are further reduced, and the depletion is virtually eliminated.

Furthermore, although shown having planar sides in Figure 1 for clarity, in an embodiment where the electrode 12 is a barrier electrode, the electrode 16 may be formed with a

30   rough or bumpy surface to increase its surface area. One conventional material that is suitable to form such a rough electrode 16 is hemispherical silicon grain (HSG) polysilicon. Also, the dielectric 14 and electrode 12 are formed such that they conform to the adjacent rough surface of the electrode 16, and thus also have increased surface areas. Therefore, the increased surface

5   areas of the electrodes 12 and 13 and the dielectric 14 increase the capacitance of the capacitor 10.

In yet another embodiment, the capacitor 10 can be used as an antifuse. As previously discussed, an antifuse is a programmable, nonvolatile device that is normally electrically open but can be programmed to become electrically closed, i.e., a short circuit. For

10   example, referring to the capacitor 10, to form one or more short circuits 18, a sufficient voltage is applied across the electrodes 12 and 16 so as to cause the dielectric 14 to break down and the short circuit 18 to develop between the electrodes 12 and 16. Because the electrode 16 is a barrier electrode, the series resistance of such an antifuse is significantly reduced as is the time constant associated with the antifuse. Therefore, circuitry coupled to the antifuse can operate at a

15   higher speed than with a conventional, higher-resistance antifuse.

Figure 2 is a cross-sectional view of a DRAM capacitor 20 according to another embodiment of the invention. The capacitor 20 includes a first electrode 22, which may be one continuous layer or may include separate layers 24a and 24b. A first barrier layer 26 is disposed adjacent to one side of the electrode 22, a conventional dielectric 28 is disposed adjacent to an

20   opposite side of the barrier layer 26, a second barrier layer 30 is disposed adjacent to another side of the dielectric 26, and a second electrode 32 is adjacent to an opposite side of the barrier layer 30. Like the first electrode 22, the second electrode 32 may be one continuous layer or may include separate layers 34a and 34b. Furthermore, like the barrier electrode 16 of Figure 1, the barrier layers 26 and 30 may be formed from conventional barrier materials such as a titanium

25   nitride, or may be formed from tungsten nitride, tungsten silicon nitride, or titanium silicon nitride. The barrier layers 26 and 30, however, can be formed such that they do not form a silicide with the adjacent electrodes 22 and 32, respectively. Alternatively, one or both of the layers 24b and 34a may be silicide layers, or respective silicide layers may be disposed between the layers 24b and 34a and the dielectric 28. Additionally, although described as used in a

30   DRAM, the capacitor 20 may be used in other applications as well.

As discussed above in conjunction with the barrier electrode 16 of Figure 1, the barrier layers 26 and 30 reduce the leakage, depletion, series resistance, and thickness of the capacitor 20 as compared with conventional capacitors, and thus allow the capacitor 20 to be

5   significantly smaller than conventional capacitors. For example, by increasing the barrier to electron flow through both sides of the dielectric 28, the barrier layers 26 and 30 significantly reduce the leakage of the capacitor 20. Furthermore, where one or both of the electrodes 22 and 32 are formed from polysilicon or another semiconductor material, the respective barrier layers 26 and 30 (having respective thicknesses as low as 10 to 100 Å in one embodiment) allow the

10   respective thicknesses of the electrodes 22 and 32 to be reduced from approximately 600 Å (the typical thickness of a conventional semiconductor electrode as discussed above in conjunction with Figure 1) to approximately 200 Å. Thus, not only does this reduction in thickness reduce the overall thickness of the capacitor 20, it also significantly reduces or eliminates the depletion that occurs in the electrodes 22 and 32. Additionally, by providing conductive paths along the

15   sides of the semiconductor electrodes 22 and 32, respectively, the barrier layers 26 and 30 allow the charge carriers within the electrodes 22 and 32 to more easily travel from one location to another, and thus significantly reduce the series resistance of the capacitor 20.

In another embodiment, one or both of the electrodes 22 and 32 may be formed from silicon germanium, which, as discussed above in conjunction with the capacitor 10 of

20   Figure 1, further reduces the leakage of the capacitor 20. Alternatively, the layers 22 and 32 may each include a layer of silicon germanium and a layer of another conductive material such as polysilicon. That is, for example, one of the layers 24a and 24b may be formed from silicon germanium and the other layer 24a and 24b formed from a conductive material such as polysilicon. Likewise, one of the layers 34a and 34b may be formed from silicon germanium,

25   and the other layer 34a and 34b formed from another conductive material such as polysilicon.

Also, as discussed above in conjunction with Figure 1, although shown having planar edges for clarity, in one embodiment, one or both of the electrodes 22 and 32 are formed with rough edges to increase their respective surface areas, thus increasing the capacitance of the capacitor 20. For example, the electrode 22, the electrode 32, or both may be formed entirely

30   from HSG polysilicon, or one of the layers 24a and 24b of the electrode 22 or one of the layers and 34a and 34b of the electrode 32 may be formed from HSG polysilicon, and the other one of the respective layers 24a and 24b, and 34a and 34b, may be formed from silicon germanium or another conductive material.

In yet another embodiment, the capacitor 20 can be used as an antifuse as discussed above for the capacitor 10 of Figure 1.

Figure 3 is a cross-sectional view of a transistor 40 according to another embodiment of the invention. The transistor 40 includes conventional source/drain regions 42 and 44, which are disposed in a substrate 46, a channel region 48, which is disposed in the substrate 46 between the source/drain regions 42 and 44, a conventional gate insulator 50, and a gate conductor 52, which includes a first conductive layer 54, a conductive barrier layer 56, and a second conductive layer 58. In one embodiment, the conductive layers 54 and 58 are formed from conventional materials. For example, the layer 54 may be a silicide layer and the layer 58 may be a polysilicon layer.

The barrier layer 56 prevents a dopant from diffusing from the layer 54, through the layer 58, and into the layer 50 during processing of the transistor 40. Where the layer 58 is a semiconductor material such as polysilicon, such diffusion can degrade the gate oxide 50 by causing mobile trapped charges that change the characteristics of the transistor 40, such as the threshold, and thus cause the transistor 40 to operate improperly for its intended use.

Because, as discussed above, conventional barrier materials such as tungsten silicide and titanium nitride are often not suited for the smaller geometries of today's denser integrated circuits, the barrier layer 56 is formed from tungsten nitride, tungsten silicon nitride, or titanium silicon nitride. These materials provide many advantages over conventional barrier materials. For example, the silicon component of tungsten silicon nitride and titanium silicon nitride allows transistor formation using a conventional "no spacer" process flow, which includes fewer steps and thus is cheaper to implement than other types of process flows. Furthermore, the silicon component of tungsten silicon nitride and titanium silicon nitride also increases the step coverage of these barrier materials as published by P.M. Smith et al., Chemical Vapor Deposition of Titanium-Silicon-Nitride Films, Applied Physics Letter 70 (23), American Institute of Physics, 9 June 1997, pp. 3116-118. Although important at any geometry, step coverage becomes more important as the geometries shrink in size. Additionally, tungsten nitride, tungsten silicon nitride, and titanium silicon nitride are more compatible with conventional polysilicon electrodes, word lines, and interconnects than are tungsten silicide and titanium nitride.

5 Moreover, because tungsten nitride, tungsten silicon nitride, and titanium silicon nitride have relatively high crystallization temperatures, they retain their barrier properties even after thermal cycling.

Figure 4 is a schematic diagram of a conventional DRAM cell 60, which includes a capacitor 62 and an access transistor 64. In one embodiment, the capacitor 42 has the same

10 structure as either the capacitor 10 of Figure 1 or the capacitor 20 of Figure 2 and the transistor 64 is conventional. In another embodiment, the capacitor 62 is conventional and the transistor 64 has the same structure as the transistor 40 of Figure 3. In yet another embodiment, the capacitor 42 has the same structure as either the capacitor 10 of Figure 1 or the capacitor 20 of Figure 2, and the transistor 64 has the same structure as the transistor 40 of Figure 3. The access transistor

15 64 has an access terminal 66 coupled to a digit line 68, a gate 70 coupled to a word line 72, and a storage terminal 74 coupled to a data terminal 76 of the capacitor 62. A reference terminal 78 of the capacitor 42 is coupled to a conventional cell plate (not shown) that is biased at a cell-plate voltage VCP. In one embodiment, the capacitor plate that composes the reference terminal 78 is actually integral with the cell plate. That is, the cell plate acts as the respective terminals/plates

20 78 for all of the capacitors 62 coupled thereto. Typically, VCP is half of the supply voltage that powers a circuit that includes the cell 60.

Figure 5 is a block diagram of a memory circuit 80, which can include the capacitor 10 or the capacitor 20 of Figures 1 and 2, respectively, the transistor 40 of Figure 3, the DRAM cell 60 of Figure 4, or a combination or subcombination of these components.

25 The memory circuit 80 includes an address register 82, which receives an address from an ADDRESS bus. A control logic circuit 84 receives a clock (CLK) signal, and receives clock enable (CKE), chip select (CS), row address strobe (RAS), column address strobe (CAS), and write enable (WE) signals from a COMMAND bus, and generates control signals for controlling the operation of the memory device 80. A row address multiplexer 86 receives the

30 address signal from the address register 82 and provides the row address to row-address latch-and-decode circuits 88a and 88b for one of two memory banks 90a and 90b, respectively. The memory banks 90a and 90b each include a large number of DRAM cells 60 (Figure 4) using one or more of several embodiments of the invention, as explained above. During read and write

5   cycles, the row-address latch-and-decode circuits 88a and 88b activate the word lines of the addressed rows of memory cells in the memory banks 90a and 90b, respectively. Read/write circuits 92a and 92b read data from the addressed memory cells in the memory banks 90a and 90b, respectively, during a read cycle, and write data to the addressed memory cells during a write cycle. A column-address latch-and-decode circuit 94 receives the address from the address

10   register 82 and provides the column address of the selected memory cells to the read/write circuits 92a and 92b. For clarity, the address register 82, the row-address multiplexer 86, the row-address latch-and-decode circuits 88a and 88b, and the column-address latch-and-decode circuit 94 can be collectively referred to as an address decoder.

A data input/output (I/O) circuit 96 includes a plurality of input buffers 98.

15   During a write cycle, the buffers 98 receive and store data from the DATA bus, and the read/write circuits 92a and 92b provide the stored data to the memory banks 90a and 90b, respectively. The data I/O circuit 96 also includes a plurality of output drivers 100. During a read cycle, the read/write circuits 92a and 92b provide data from the memory banks 90a and 90b, respectively, to the drivers 100, which in turn provide this data to the DATA bus.

20   A refresh counter 102 stores the address of the row of memory cells to be refreshed either during a conventional auto-refresh mode or self-refresh mode. After the row is refreshed, a refresh controller 104 updates the address in the refresh counter 102, typically by either incrementing or decrementing the contents of the refresh counter 102 by one. Although shown separately, the refresh controller 104 may be part of the control logic 84 in other

25   embodiments of the memory device 80.

The memory device 80 may also include an optional charge pump 106, which steps up the power-supply voltage VDD to a voltage VDDP. In one embodiment, the pump 106 generates VDDP approximately 1-1.5 V higher than VDD. The memory circuit 80 may also use VDDP to conventionally overdrive selected internal transistors.

30   Figure 6 is a block diagram of an electronic system 110, such as a computer system, which incorporates the memory circuit 80 of Figure 5. The system 110 includes computer circuitry 112 for performing computer functions, such as executing software to perform desired calculations and tasks. The circuitry 112 typically includes a processor 114 and the

5   memory circuit 80, which is coupled to the processor 114. One or more input devices 116, such as a keyboard or a mouse, are coupled to the computer circuitry 112 and allow an operator (not shown) to manually input data thereto. One or more output devices 118 are coupled to the computer circuitry 112 to provide to the operator data generated by the computer circuitry 112. Examples of such output devices 118 include a printer and a video display unit. One or more

10   data-storage devices 120 are coupled to the computer circuitry 112 to store data on or retrieve data from external storage media (not shown). Examples of the storage devices 120 and the corresponding storage media include drives that accept hard and floppy disks, tape cassettes, and compact disk read-only memories (CD-ROMs). Typically, the computer circuitry 112 includes address data and command buses and a clock line that are respectively coupled to the

15   ADDRESS, DATA, and COMMAND buses, and the CLK line of the memory device 80.

Figure 7 is a cross-sectional view of a conventional semiconductor structure 700 including a memory cell 701, which comprises a transistor 703 electrically coupled to a capacitor 705 via a plug 718. The transistor 703 is built on a substrate 702 and is isolated from other transistors (not shown) by a field oxide layer 704. The transistor 703 includes highly doped areas

20   706 that act as source or drain regions, and also includes a gate stack 707, which controls the flow of charge carriers through a chanel region 709 defined between the highly doped areas 706. The gate stack 707 includes a gate oxide layer 708, a polycrystalline silicon gate layer 710, a silicide layer 712, a gate cap layer 714, and spacers 716.

A nonconductive layer 720 electrically isolates the transistor 703 and structurally

25   supports the capacitor 705, and non-conductive layer 722 surrounds the capacitor 705 to electrically isolate it from other semiconductor devices (not shown). The capacitor 705 comprises a substrate 724, which may be made from polysilicon-germanium; a hemispherical silicon grain (HSG) layer 726 is formed adjoining the substrate 724, and may be formed from a germanium-doped amorphous silicon layer. The substrate 724 together with the HSG layer 726

30   forms a bottom electrode 727 of the capacitor 705. A dielectric layer 728 is formed conforming to the HSG layer 726, and a top electrode layer 730 is formed on the dielectric layer 728.

As previously discussed with reference to Figures 1 and 2, the HSG layer 726 increases the surface areas of the bottom electrode 727 and top electrode layer 730 of capacitor

5 705, and hence, increases its capacitance. The significance of this increased surface areas by the HSG layer 726 may be understood by revisiting the physics of a capacitor in the context of the trend of ongoing miniaturization of semiconductor devices: A measure of the ability of the capacitor to store charge is called capacitance. The capacitance is given by $\varepsilon A/d$, where ε is the permittivity of the dielectric, A is the area of the electrodes, and d is the distance separating the

10 electrodes. Both the area A and the distance d of the capacitor define the physical dimensions of the capacitor, and as the area A increases the capacitance, the ability of the capacitor to store charge also increases.

Capacitors of memory cells are built in limited space so as to comport with the ongoing trend of miniaturization of semiconductor devices. Even with such physical constraints,

15 the capacitance of these capacitors must be kept high to store sufficient charge and avoid excessive dissipation of charge over time. One technique to raise the capacitance is to increase the area A by roughening the surface of an electrode of the capacitor. This roughening process forms hemispherical protrusions (or grains) that protrude from the surface of the electrode. The curvature surface of each grain provides a greater area than the flat surface of the electrode from

20 which each grain protrudes. Thus, the combined surface areas of the grains increase the area A of the electrode and thereby raise the capacitance of the capacitor.

The resulting roughened surface is also known as an HSG (hemispherical silicon grain) layer. While the HSG layer helps to increase capacitance, a further increase in capacitance may be desired as the space in which the capacitor is formed continues shrinking. Moreover,

25 during formation of the HSG layer 726, atoms in a previously deposited layer are consumed to form the hemispherical protrusions and thereby form the HSG layer, as will be understood by those skilled in the art. Atoms in the underlying electrode layer 724 may also be consumed during formation of the HSG layer 726. Unwanted holes in the HSG layer 726 and electrode layer 724 may result as such atoms are consumed from each layer, and such holes can allow

30 underlying regions to be damaged during subsequent processing steps. This limits the ability to form large hemispherical protrusions on the layer 726 to increase the area of the layer.

Figure 8 is a cross-sectional view of a semiconductor structure 800 according to one embodiment of the present invention. The semiconductor structure 800 includes a memory

5   cell 801A, which comprises a transistor 803A coupled through the corresponding plug 718 to a capacitor 805A, and a memory cell 801B, which comprises a transistor 803B coupled through the corresponding plug 718 to a capacitor 805B. Some of the structural details and components of the memory cells 801A and 801B are similar to those discussed with reference to Figure 7, and for the sake of brevity, such components have been given the identical reference numerals as

10   corresponding components in Figure 7. These components and structural details will not again be discussed in detail.

    In Figure 8, the capacitor 805A includes a first polycrystalline electrode layer 824 formed to contact the corresponding plug 718 and an HSG layer 826 formed on an inner surface 825 of the first polycrystalline electrode layer. The first polycrystalline electrode layer 824 and

15   HSG layer 826 together form a bottom electrode 827 of the capacitor 805A. The first polycrystalline electrode layer 824 prevents damage to underlying regions if openings or perforations in the HSG layer 826 occur during formation of that layer, as will be described in more detail below. In one embodiment, the HSG layer is formed from an undoped amorphous silicon layer, as will be discussed in more detail below. In the structure 800, some of the

20   nonconducting layer 722 is removed to expose an outer surface 829 of the electrode layer 824, and the HSG layer 826 is also formed on the outer surface 829. A dielectric layer 828 is then formed on the HSG layer 826 and on an upper portion 831 of the electrode layer 824. A top electrode layer 830 is formed on the dielectrode layer 828. Each of the layers 826-830 may be formed from the same materials as the corresponding layers in the structure of Figure 7 or other

25   suitable materials as will be understood by those skilled in the art. The capacitor 805B has the same structure as that just described for the capacitor 805A, and thus, for the sake of brevity, will not be described in more detail. The capacitors 805A and or 805B have increased respective capacitance values due to the increased areas of the bottom electrode 827 and top electrode layer 830. The use of both the inner and outer surfaces of the first polycrystalline electrode layer 824

30   along with the HSG layer 826 deposited thereon increases the surface area of the bottom electrode 827 which, in turn, increases the surface areas of the dielectric layer 828 and top electrode layer 830. Thus, the capacitors 805A, 805B have increased capacitance values relative

5   to the conventional capacitors 705 due to the increased areas of the bottom electrode 827 and top electrode layer 830.

Figure 9 is a cross-sectional view of a semiconductor structure 900 according to another embodiment of the present invention. The semiconductor structure 900 includes a memory cell 901A, including a transistor 903A coupled to a capacitor 905A, and a memory cell

10   901B including a transistor 903B coupled to a capacitor 905B. Some of the structural details and components of the memory cells 901A and 901B are similar to those discussed in Figure 8, and for the sake of brevity, such components have been given identical reference numerals, as corresponding components in Figure 8. These components and structural details will not again be discussed in detail.

15   The capacitors 905A and 905B are identical, and thus only the capacitor 905A will be discussed in more detail. In the embodiment of Figure 9, the capacitor 905A once again includes the first electrode layer 824 formed to contact the corresponding plug 718 and an HSG layer 926 formed on the inner surface 825 of the first electrode layer. A portion of the nonconductive layer 722 is again removed to expose an outer surface 829 of the first

20   polycrystalline electrode layer 824. A dielectric layer 928 is then formed at the outer surface 829 and on the upper portion 831 of the first polycrystalline electrode layer 824, and is also formed on the HSG layer 926. A top electrode layer 930 is then formed on the dielectric layer 928. In the capacitor 905A, the first polycrystalline electrode layer 824 and HSG layer 926 form a bottom electrode 927 of the capacitor. The bottom electrode 927 and top electrode layer 930

25   have increased areas relative to the bottom electrode 727 and top electrode layer 730 in the conventional capacitor 705 of Figure 7. These increased areas are due to the area added by the use of the outer surface 829 of the first electrode layer 824. By omitting the formation of the HSG layer 926 on the outer surface 829 of the layer 824, the structure of the capacitor 905A provides an increased capacitance while having a relatively small width W, which allows the

30   capacitors 905A, 905B to be more densely formed, as will be appreciated by those skilled in the art.

Figures 10A-10K are cross-sectional views of the semiconductor structure 900 during processing according to one embodiment of the present invention. Figures 10A-10G

illustrate the formation of the HSG layer 926 via an in-situ processing technique while Figures 10H-10K illustrate the formation of the HSG layer via an ex-situ processing technique. The discussion in Figures 10A-10K illustrates a few of the steps associated with a sample fabrication process. The entire fabrication process is not discussed so as to focus on the embodiments of the present invention, and one skilled in the art will understand such overall fabrication processes and appreciate various other methods of fabrication that may be utilized in forming the structures 800 and 900. One skilled in the art will also appreciate various fabrication processes that may be utilized in forming the capacitor 805A, 805B and the structure 800 of Figure 8. For the sake of clarity, many of the reference numbers in Figures 10A-10K, once discussed, may be eliminated from subsequent drawings.

In the in-situ process of Figures 10A-10G, Figure 10A is a cross-sectional view of the semiconductor structure 900 during processing and illustrates that the nonconductive layer 722 is etched to form openings 1000A and 1000B, each opening defining a container, which will house a corresponding capacitor 905A, 905B. The other semiconductor elements in Figure 10A, such as the transistors 703 and plugs 718, are formed using conventional techniques, and thus their formation will not be described in detail. Briefly, the gate oxide 708 is grown over the channel region 707 of the substrate 702, which can be formed from any suitable substance, such as lightly doped n-type or p-type material and a lightly doped epitaxial layer on a heavily doped substrate. The field oxide layer 704 may be deposited, patterned, and etched on the substrate 702 and the polycrystalline silicon gate 710 formed by depositing a polycrystalline silicon layer over the gate oxide layer 708 and then photolithographed and etched appropriately. Impurities of the appropriate kind are implanted or otherwise introduced into the substrate 702 to form the highly doped source and drain regions 706. The silicide layer 712 is formed on the polycrystalline silicon gate 710 to create a metal/semiconductor junction. The gate cap layer 714 and spacers 716 are formed by depositing a dielectric layer which is then photolithographed and etched. The nonconductive layer 720 is formed over these components and the plugs 718 are formed in the nonconductive layer to electrically contact the highly doped areas 706. The nonconductive layer 722, such as borophosphorus silicate glass (BPSG), is deposited over the nonconductive layer 720.

5   Figure 10B is a cross-sectional view of the semiconductor structure 900 during the

next sequence of in-situ processing in which a conductive layer 1002 is deposited over the

nonconductive layer 722 and into the openings 1000A and 1000B. The conductive layer 1002

can be of any suitable material that will form a polycrystalline structure so that the majority of

atoms are sufficiently bound to resist being drawn out of the layer 1002 and contributing to the

10   formation of the HSG layer 926, as will be discussed in more detail hereinbelow. This

conductive layer 1002 will be part of the bottom electrode 927 of the two capacitors 905A, 905B,

housed in the openings 1000A and 1000B, respectively. One suitable material for the layer 1002

includes a silicon-germanium alloy. The deposition process of the silicon-germanium alloy

includes low-pressure chemical-vapor deposition, which forms the silicon-germanium alloy to a

15   thickness of less than about 500 angstroms. In such a deposition process, at a temperature greater

than about 500 degrees Celsius, silane gas (Si_nH_{2n+2}) is allowed to flow along with phosphine gas

(PH_3) and digermanium hexahydride (Ge_2H_6) or germanium tetrahydride (GeH_4) on the surface

of the nonconductive material 722 including the openings 1000A and 1000B. The silicon-

germanium alloy will become polycrystalline at about 500 degrees Celsius during this sequence

20   of processing. Because of the transformation the layer 1002 from the silicon-germanium alloy to

a polycrystalline structure, the conductive layer 1002 is also designated 824, which is the

reference number used to refer to this polycrystalline electrode layer in Figures 8 and 9.

Figure 10C is a cross-sectional view of the semiconductor structure 900 during the

next sequence of in-situ processing. After the transformation of the silicon-germanium alloy

25   1002 into the polycrystalline electrode layer 824, silane gas is again allowed to flow to deposit an

undoped amorphous silicon layer 1004 at an appropriate temperature. In one embodiment, the

temperature is less than about 550 degrees Celsius, in another embodiment the temperature is

less than about 450 degrees Celsius, and in yet another embodiment the temperature is about 300

degrees Celsius. This deposition process forms the undoped amorphous silicon layer 1004 at a

30   thickness less than about 500 angstroms.

Figure 10D is a cross-sectional view of the semiconductor structure 900 during

the next sequence of in-situ processing in which the undoped amorphous silicon layer 1004

undergoes a seeding process to form a number of seeds 1006 on the surface of the undoped

5   amorphous silicon layer 1004. The seeding process begins by bathing the surface of the undoped amorphous silicon layer 1004 in silane gas at a flow rate greater than about 10 standard cubic centimeters per minute and less than about 30 standard cubic centimeters per minute. The temperature should be raised to greater than about 550 degrees Celsius and less than about 600 degrees Celsius. The seeding process is a precipitation of solids from a gaseous matrix to form

10   the seed 1006. Nucleation is the first step of the seeding process, and it describes the clustering of silicon atoms on the surface of the undoped amorphous silicon layer 1004 to randomly produce many nuclei or seeds 1006. Those seed 1006 that are larger than a certain size are stable and as a result can participate in the growing process, which will be described in more detail below.

15   Figure 10E is a cross-sectional view of the semiconductor structure 900 during the next sequence of in-situ processing in which the semiconductor structure 900 undergoes an annealing process, which causes the seeds 1006 (Figure 10D) to grow into hemispherical protrusions and thereby transform the layer 1004 and seed 1006 into the HSG layer 926. The annealing process is at a temperature that allows silicon atoms from the undoped amorphous

20   silicon layer 1004, which are within the vicinity of the seeds 1006, to be drawn into the seeds 1006. As more and more silicon atoms are drawn into the seeds 1006, the seeds 1006 begin to grow and forms the hemispherical protrusions on the HSG layer 926 as discussed above. The annealing process preferably occurs for about 30 minutes at a temperature greater than about 550 degrees Celsius and less than about 600 degrees Celsius.

25   Depending on the thickness of the undoped amorphous silicon layer 1004, too many of the atoms from the undoped amorphous silicon layer 1004 may participate in the growing of the hemispherical protrusions, and thus, may lead to the formation of undesired perforations in the HSG layer 926. The perforations may allow etching solutions, which are used in subsequent processing steps, to leak through and damage underlying components of the

30   semiconductor structure 900. Because of the presence of the polycrystalline layer 824, however, even if such perforations in the HSG layer 926 occur, the polycrystalline layer 824 protects the semiconductor structure 900 from any damage due to the leakage of etchant solutions through the perforations. The atoms in the polycrystalline layer 824, as explained above, are bound

5   sufficiently in the layer 824 so that most of the atoms will not be drawn into the HSG layer 926 during the growing of the hemispherical protrusions on the HSG layer 926. Thus, the polycrystalline layer 824 remains intact during the annealing process so as to provide a protective barrier should undesired perforation of the HSG layer 926 occur.

Figure 10F is a cross-sectional view of the semiconductor structure 900 during the

10   next sequence of in-situ processing in which the semiconductor structure 900 as shown in Figure 10E undergoes a chemical-mechanical planarization process to remove portions of the HSG layer 926 and layer 824. The planarization process removes the HSG layer 926 except for the portions of that layer in the openings 1000A and 1000B, and also removes most of the polycrystalline layer 824. The structure resulting after the chemical-mechanical planarization process is

15   illustrated in Figure 10F.

Figure 10G is a cross-sectional view of the semiconductor structure 900 during the next sequence of in-situ processing in which the semiconductor structure 900 is photolithographed and etched so that most of the nonconductive layer 722 is removed to expose the outer surfaces 829 of the polycrystalline electrode layer 824 as shown. The etching process

20   includes an etch-back process, which uses an etching solution formed from a 10:1 ratio of water to hydrofluoric acid. The remaining steps to complete the formation of the capacitors 905A and 905B are conventional, and thus, for the sake of brevity, will not be described in detail. For example, the deposition of the dielectric layer 928 (See Figure 9) over the HSG layer 926 is followed by a deposition of a conductive material over the dielectric layer to form the top

25   electrode layer 930 to complete the formation of the capacitors 905A, 905B of Figure 9.

What has been discussed with reference to Figures 10A-10G involves the formation of the HSG layer 926 via an in-situ process. What will be discussed below with reference to Figures 10H-10K illustrates the formation of the HSG layer 926 via an ex-situ process. The ex-situ process begins similarly to the in-situ process with the formation of the

30   openings 1000A and 1000B as discussed in Figure 10A, which is followed by the formation of the conductive layer 1002 as discussed in Figure 10B, and the formation of the undoped amorphous silicon layer 1004 as discussed in Figure 10C. The similarity between the in-situ and ex-situ processes ends there.

5   The ex-situ process of forming the HSG layer 926 is shown in Figures 10H-10K. Figure 10H is a cross-sectional view of the semiconductor structure 900 during a sequenece of ex-situ processing in which the semiconductor structure 900 of Figure 10C undergoes a chemical-mechanical planarization process to remove the polycrystalline layer 824 and the undoped amorphous silicon layer 1004 except for the portions of these layers in the openings

10   1000A and 1000B.

       Figure 10I is a cross-sectional view of the semiconductor structure 900 during the next sequence of ex-situ processing in which the semiconductor structure of Figure 10H is photolithographed and etched to remove most of the nonconductive layer 722 and expose the outer surfaces 829 of the polycrystalline electrode layer 824. The etching process includes an

15   etch-back process, which uses an etching solution formed from a 10:1 ratio of water to hydrofluoric acid.

       The next step of the ex-situ process is shown in Figure 10J, which illustrates a seeding process being applied to form a number of seeds 1006 on the surface of the undoped amorphous silicon layer 1004. The undoped amorphous silicon layer 1004 is bathed in silane gas

20   at a flow rate greater than about 15 standard cubic centimeters per minute. The temperature should be raised to greater than about 600 degrees Celsius and less than about 650 degrees Celsius. Because the outer surfaces 829 of the polycrystalline layer 824 are exposed, the seeds 1006 are formed on both the surfaces of the undoped amorphous silicon layer 1004 and on the surfaces of the polycrystalline layers 824.

25   Figure 10K shows the next sequence of the ex-situ process in which the semiconductor structure 900 undergoes a high-vacuum annealing process so as to grow the seeds 1006 as shown in Figure 10J into hemispherical protrusions and thereby form the HSG layers 926. In one embodiment, the annealing process occurs for about five minutes at a temperature greater than about 600 degrees Celsius and less than about 650 degrees Celsius. As discussed

30   above, the atoms in the polycrystalline layer 824 are sufficiently bound in the layer 824 so that most of the atoms will not participate in the growing of the hemispherical protrusions. As a result, the seeds 1006 on the surface of the polycrystalline layer 824 are unlikely to grow significantly, and the surface of the polycrystalline layer 824 remains relatively smooth. The

5   polycrystalline layer 824 once again acts as a protective barrier to protect regions underlying the layer 824 should undesired perforation of the HSG layer 926 occur. The remaining steps to complete the formation of the capacitors 905A and 905B are conventional, and thus will not be described in detail. For example, the deposition of the dielectric layer 928 (Figure 9) over the HSG layer 926 is followed by a deposition of a conductive material over the dielectric layer to

10   form as the top electrode layer 930 and complete the formation of the capacitors 905A, 905B of Figure 9.

        From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention

15   is not limited except as by the appended claims.